What Is Claimed Is:

1. A method of integrated circuit repair comprising:

removing the top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a wet chemistry process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

etching a selected portion of a metal interconnect using a FIB.

2. The method of Claim 1 wherein said top dielectric layer is a protective overcoat layer.

3. The method of Claim 1 wherein said top metal layer is a power bus layer.

4. The method of Claim 1 wherein said step of etching selected portions of one or more dielectric interconnect layers using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

5. The method of Claim 1 wherein said step of removing the top dielectric layer in at least one location using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

6. The method of Claim 1 wherein said wet chemistry process uses a hood.

7. The method of Claim 1 wherein said step of etching a selected portion of a metal interconnect using a FIB includes the use of a Gallium liquid metal ion source and Xenon DiFluoride gas.

8. The method of Claim 1 wherein said wet chemistry process includes the use of Nitric Acid.

9. The method of Claim 1 wherein said top metal layer contains copper.

10. The method of Claim 1 wherein said metal interconnect contains copper.

11. A method of integrated circuit repair comprising:

removing the top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a plasma etch process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

etching a selected portion of a metal interconnect using a FIB.

12. A method of integrated circuit repair comprising:

removing the top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a wet chemistry process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

coupling a first metal interconnect portion to a second metal interconnect portion using a FIB.

13. The method of Claim 12 wherein said first metal interconnect portion and said second metal interconnect portion are located in the same metal interconnect layer.

14. The method of Claim 12 wherein said first metal interconnect portion and said second metal interconnect portion are located in different metal interconnect layers.

15. The method of Claim 12 wherein said coupling a first metal interconnect portion to a second metal interconnect portion using a FIB includes the use of a Gallium LMI beam source and Platinum conductive gas.

16. The method of Claim 12 wherein said top dielectric layer is a protective overcoat layer.

17. The method of Claim 12 wherein said top metal layer is a power bus layer.

18. The method of Claim 12 wherein said step of etching selected portions of one or more dielectric interconnect layers using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

19. The method of Claim 12 wherein said step of removing the top dielectric layer in at least one location using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

20. The method of Claim 12 wherein said wet chemistry process uses a hood.

21. The method of Claim 12 wherein said wet chemistry process includes the use of Nitric Acid.

22. The method of Claim 12 wherein said top metal layer includes copper.

23. The method of Claim 12 wherein said first metal interconnect and said second metal interconnect includes copper.

24. A method of integrated circuit repair comprising:

removing the top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a plasma etch process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

coupling a first metal interconnect portion to a second metal interconnect portion using a FIB.

25. A method of integrated circuit repair comprising:

forming a top dielectric layer over said integrated circuit;

removing said top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a wet chemistry process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

etching a selected portion of a metal interconnect using a FIB.

26. The method of Claim 25 wherein said top dielectric layer is formed using a PVD process.

27. The method of Claim 25 wherein said top dielectric layer is formed using a CVD process.

28. The method of Claim 25 wherein said top metal layer is a BOAC layer.

29. The method of Claim 25 wherein said step of etching selected portions of one or more dielectric interconnect layers using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

30. The method of Claim 25 wherein said step of removing said top dielectric layer in at least one location using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

31. The method of Claim 25 wherein said wet chemistry process uses a hood.

32. The method of Claim 25 wherein said step of etching a selected portion of a metal interconnect using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

33. The method of Claim 25 wherein said wet chemistry process includes the use of Nitric Acid.

34. The method of Claim 25 wherein said top dielectric layer includes Silicon Nitride.

35. The method of Claim 25 wherein said top metal layer contains copper.

36. The method of Claim 25 wherein said metal interconnect contains copper.

37. A method of integrated circuit repair comprising:

forming a top dielectric layer over said integrated circuit;

removing the top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a plasma etch process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

etching a selected portion of a metal interconnect using a FIB.

38. A method of integrated circuit repair comprising:

forming a top dielectric layer over said integrated circuit;

removing the top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a wet chemistry process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

coupling a first metal interconnect portion to a second metal interconnect portion using a FIB.

39. The method of Claim 38 wherein said first metal interconnect portion and said second metal interconnect portion are located in the same metal interconnect layer.

40. The method of Claim 38 wherein said first metal interconnect portion and said second metal interconnect portion are located in different metal interconnect layers.

41. The method of Claim 38 wherein said coupling a first metal interconnect portion to a second metal interconnect portion using a FIB includes the use of a Gallium LMI beam source and Platinum conductive gas.

42. The method of Claim 38 wherein said top dielectric layer is formed using a PVD process.

43. The method of Claim 38 wherein said top dielectric layer is formed using a CVD process.

44. The method of Claim 38 wherein said top metal layer is a BOAC layer.

45. The method of Claim 38 wherein said step of etching selected portions of one or more dielectric interconnect layers using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

46. The method of Claim 38 wherein said step of removing the top dielectric layer in at least one location using a FIB includes the use of a Gallium LMI source and Xenon DiFluoride gas.

47. The method of Claim 38 wherein said wet chemistry process uses a hood.

48. The method of Claim 38 wherein said wet chemistry process includes the use of Nitric Acid.

49. The method of Claim 38 wherein said top dielectric layer includes Silicon Nitride.

50. The method of Claim 38 wherein said top metal layer includes copper.

51. The method of Claim 38 wherein said first metal interconnect and said second metal interconnect includes copper.

52. A method of integrated circuit repair comprising:

forming a top dielectric layer over said integrated circuit;

removing the top dielectric layer in at least one location using a FIB;

etching exposed areas of a top metal layer using a plasma etch process;

etching selected portions of one or more dielectric interconnect layers using a FIB; and

coupling a first metal interconnect portion to a second metal interconnect portion using a FIB.